## WHAT IS CLAIMED IS:

1	1.	A Programmable Logic Device (PLD) incorporating a plurality of		
2	Programmable Logic Blocks (PLBs) providing enhanced flexibility for Cascade logic			
3	functions, each comprising:			
4	-	a multi-input Look Up Table (LUT) providing one input to a Cascade		
5		Logic block for implementing desired Cascade Logic functions		
6		receiving a Cascade-In input as the other input, and		
7	-	a 2-input selection multiplexer receiving one input from the output of		
8		the Cascade Logic block and the other from the output of the LUT for		
9		selecting either the Cascade Logic output or the LUT output as the		
0		unregistered output,		
1	the a	rrangement being such that the output of the cascade logic and the		
2	unregistered	d output are simultaneously available, as separate outputs of the PLB		
1	2.	A Programmable Logic Device (PLD) as claimed in claim 1, further		
2	including a 2-input Cascade input multiplexer for selecting the Cascade-In signal in			
3	either its inverted or non-inverted form as one input to the Cascade Logic.			
1	3.	A Programmable Logic Device (PLD) as claimed in claim 1, wherein		
2	the PLB includes:			
3	-	a flip flop connected to the output of the selection multiplexer for		
4		providing registered output, and		
5	-	a 2-input output multiplexer for selecting either the unregistered output		
6		or the registered output as the final output of the PLB		
1	4.	A Programmable Logic Device (PLD) as claimed in claim 1 wherein the		
2	PLB includes a feedback arrangement for connecting the final output to the input of			
3	the LUT to enhance the flexibility of the Cascade Logic as well as the normal			
4	functions of the PLB.			
1	5.	A method for enhancing the flexibility of Cascade Logic functions in the		
2	Programmable logic Block (PLB) of a Programmable Logic Device (PLD), comprising			
3	the steps of:			
4	-	providing a 2-input selection multiplexer for receiving one input from		
5		the output of the Cascade Logic block and the other from the output of		

0		the LOT and selecting either the Cascade Logic output of the LOT	
7		output as the unregistered output, and	
8	-	providing simultaneous access to the cascade logic output and the	
9		unregistered output as separate outputs of the PLB for use as sub	
10		functions in cascade logic or in other logic functions.	
1	6.	A method as claimed in claim 5, further including the steps of:	
2	-	providing a flip flop connected to the output of the selection multiplexe	
3		for providing registered output, and	
4	-	providing a 2-input output multiplexer for selecting either the	
5		unregistered output or the registered output as the final output of the	
6		PLB.	
1	7.	A method as claimed in claim 5 further including the step of providing	
2	an arrangement for feedback of the final output to the input of the LUT to enhance		
3	the flexibility	of the Cascade Logic as well as the normal functions of the PLB	
1	8.	A method as claimed in claim 5, further including a 2-input Cascade	
2	input multiplexer for selecting the Cascade-In signal in either its inverted or non-		
3	inverted form as one input to the Cascade Logic.		
1	9.	A programmable logic block, comprising:	
2	a log	ic array operable to generate a first signal;	
3	a first cascade logic circuit coupled to the array and operable to receive a		
4	second signal from a second cascade logic circuit of another programmable logic		
5	block and to generate a third signal from the first and second signals; and		
6	a first multiplexer operable to receive the first and third signals and a first		
7	control signal and to pass either the first or third signal in response to the control		
8	signal.		
1	10.	The programmable logic block of claim 9 wherein the logic array	
2	comprises a	a look-up table.	
1	11.	The programmable logic block of claim 9 wherein the first cascade	
2	logic circuit comprises a logic gate.		
1	12.	The programmable logic block of claim 9, further comprising a flip flop	
2	that is opera	able to receive the signal passed by the multiplexer.	

	13. The programmable logic block of claim 9, further comprising.			
2	a flip flop operable to receive the signal passed by the first multiplexer and to			
3	generate a flip-flop output signal from the received signal; and			
4	a second multiplexer operable to receive the signal passed by the first			
5	multiplexer, the flip flop-flop output signal, and a second control signal, and to pass			
3	either the signal from the first multiplexer or the flip-flop output signal in response to			
7	the second control signal.			
1	14. The programmable logic block of claim 9, further comprising:			
2	a flip flop operable to receive the signal passed by the first multiplexer and to			
3	generate a flip-flop output signal from the received signal;			
4	a second multiplexer operable to receive the signal passed by the first			
5	multiplexer, the flip flop-flop output signal, and a second control signal and to pass			
6	either the signal from the first multiplexer or the flip-flop output signal in response to			
7	the second control signal; and			
8	wherein the logic array is operable to receive the signal passed by the second			
9	multiplexer.			
1	15. The programmable logic block of claim 9, further comprising a second			
2	multiplexer coupled between the first cascade logic circuit and the second cascade			
3	logic circuit and operable to receive the second signal, a complement of the second			
4	signal, and a second control signal and to pass to the first cascade logic circuit either			
5	the second signal or the complement of the second signal in response to the second			
6	control signal.			
1	16. The programmable logic block of claim 9, further comprising:			
2	an output node; and			
3	wherein the first multiplexer is operable to pass the first or third signal to the			
4	output node.			
1	17. An integrated circuit, comprising:			
2	a first programmable logic block having a first cascade logic circuit operable to			
3	generate a first signal; and			
4	a second programmable logic block comprising,			
5	a logic array operable to generate a second signal.			

6	a second cascade logic circuit coupled to the first programmable logic		
7	block and to the logic array and operable to generate a third signal from the		
8	first and second signals, and		
9	a multiplexer operable to receive the second and third signals and a		
10	control signal and to pass either the second or third signal in response to the		
11	control signal.		
1	18. An electronic system, comprising:		
2	an integrated circuit, comprising,		
3	a first programmable logic block having a first cascade logic circuit		
4	operable to generate a first signal, and		
5	a second programmable logic block comprising,		
6	a logic array operable to generate a second signal,		
7	a second cascade logic circuit coupled to the first programmable		
8	logic block and to the logic array and operable to generate a third		
9	signal from the first and second signals, and		
10	a multiplexer operable to receive the second and third signals		
11	and a control signal and to pass either the second or third signal in		
12	response to the control signal.		
1	19. The electronic system of claim 18 wherein the integrated circuit		
2	comprises a programmable logic device.		
1	20. The electronic system of claim 18 wherein the integrated circuit		
2	comprises a field-programmable gate array.		
1	21. A method, comprising:		
2	generating a first signal with a first cascade logic circuit of a first		
3	programmable logic block;		
4	generating a second signal with a logic array of a second programmable logic		
5	block;		
6	generating from the first and second signals a third signal with a second		
7	cascade logic circuit of the second programmable logic block; and		
8	selectively passing either the second or third signal to an output node of the		
9	second programmable logic block.		

1	22.	The method of claim 21 wherein selectively passing the second or third		
2	signal comprises passing either the second or third signal to the output node in			
3	response to a control signal.			
1	23.	A method, comprising:		
2	gene	rating a first signal with a first cascade logic circuit of a first		
3	programmable logic block;			
4	passing a second signal that is selectively equal to either the first signal or a			
5	complement of the first signal to a second cascade logic circuit of a second			
6	programmable logic block;			
7	generating a third signal with a logic array of the second programmable logic			
8	block;			
9	generating from the second and third signals a fourth signal with the second			
0	cascade logic circuit; and			
1	selectively passing either the third or fourth signal to an output node of the			
2	second programmable logic block.			
1	24.	The method of claim 23 wherein passing the second signal comprises		
2	setting the second signal equal to either the first signal or a complement of the first			
3	signal in response to a control signal.			
1	25.	A method, comprising:		
2	generating a first signal with a first cascade logic circuit of a first			
3	programmable logic block;			
4	generating a second signal with a logic array of a second programmable logic			
5	block;			
6	gene	erating from the first and second signals a third signal with a second		
7	cascade logic circuit of the second programmable logic block;			
8	selectively passing either the second or third signal; and			
9	registering the passed signal.			
1	26.	The method of claim 25, further comprising selectively passing the		
2	passed signal or the registered signal to an output node of the second			
3	programmable logic block.			

- 1 27. The method of claim 25, further comprising selectively feeding back the
- 2 passed signal or the registered signal to the logic array.